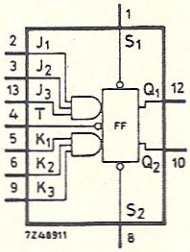
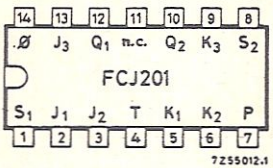
The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

development sample data

SINGLE JK MASTER-SLAVE FLIP-FLOP





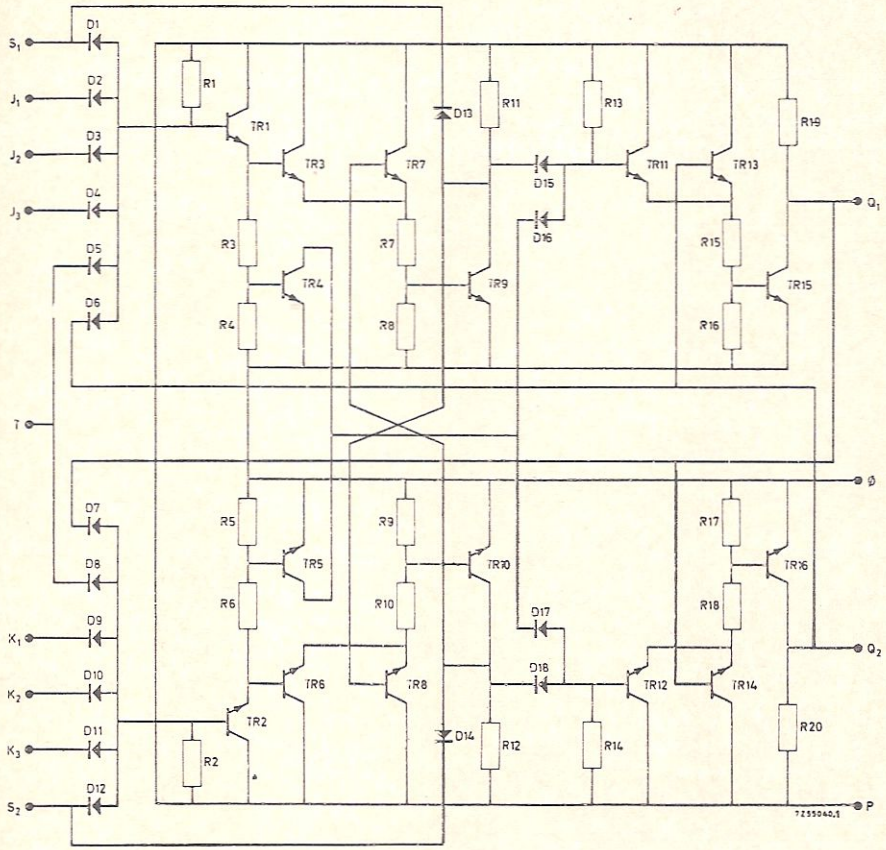
Package XG14; dual in-line

QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 5	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 67	mW

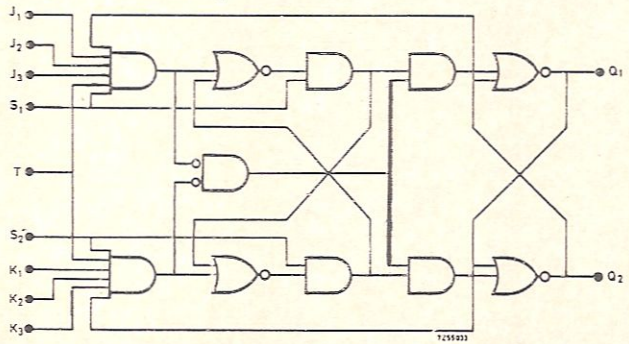
The FCJ201 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set inputs (overriding any other inputs) are active at the LOW level.

These data, based on the specifications and measured performance of development samples, afford a preliminary indication of the characteristics to be expected of the described product. Distribution of development samples implies no guarantee as to the subsequent availability of the product

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$ (for positive logic)

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S_1 and S_2 should be HIGH or floating.

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$
(for positive logic)

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

The set inputs override the other inputs and directly determine the output of the flip-flop. In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage.
3) At this limit input voltage type.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	μA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	$V_I=V_K=0.4$ V; other inp. floating
	$-I_{TLmax}$	3.5 4.0	3.3 3.8	3.1 3.6	mA mA	5.7 6.3	$V_T=0.4$ V; other inputs floating
	$-I_{SLmax}$	2.7 3.0	2.6 2.9	2.4 2.7	mA mA	5.7 6.3	$V_S=0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S, T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references		
		0	+25	+75	V_P (V)		fig.
DYNAMIC DATA					5.7 and 6.3		
Change of state							
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	3.1	2.9	2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
T-input time HIGH	t_{THmin}	100	100	100 ns			1
to: Input voltage LOW	V_{TLmax}	1.3	1.1	0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state							
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8	1.6	1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection							
Hold time	$t_{holdmax}$	20	20	20 ns			2
Set or Reset							
S input voltage LOW	V_{SLmax}	1.2	1.0	0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1	2.9	2.5 V		inactive	
DYNAMIC DATA							
Propagation delay times from T to Q							
Rise propagation delay time	t_{pdrmax}	-	200	- ns		V_{pd} = 1.5 V. N = 1; C_w = 60 pF other output N = 8; C_w = 30 pF	4
Fall propagation delay time	t_{pdfmax}	-	100	- ns		V_{pd} = 1.5 V N = 8; C_w = 30 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

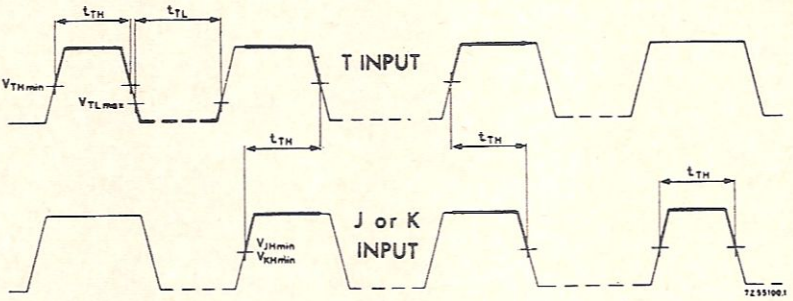


Fig. 1. Waveforms illustrating conditions for change of state.

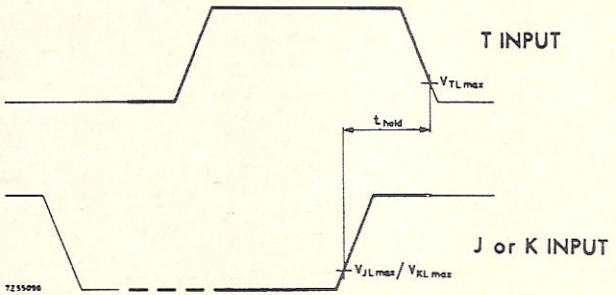


Fig. 2. Waveforms illustrating conditions for no change of state.

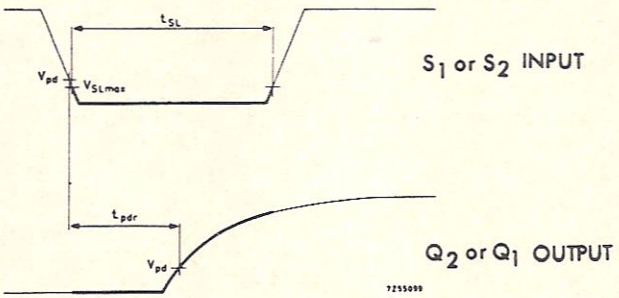
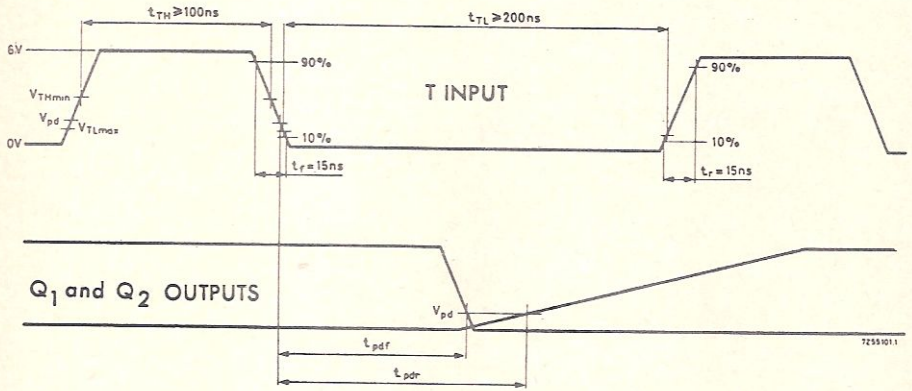
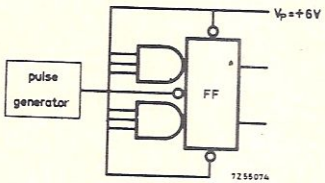


Fig. 3. Waveforms illustrating conditions for set or reset.

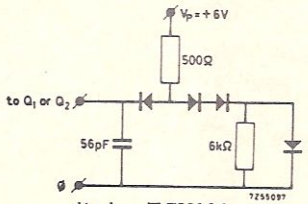
CHARACTERISTICS (continued)

DYNAMIC DATA



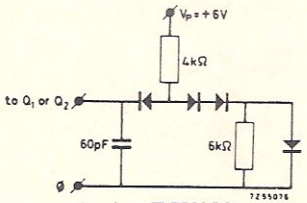


$C_L = C_W + C_i (N - 1)$



diodes FCY101

Equivalent load for N = 8 and C_W = 30 pF



diodes FCY101

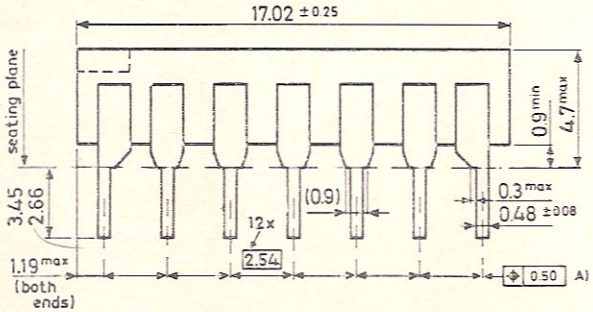
Equivalent load for N = 1 and C_W = 60 pF

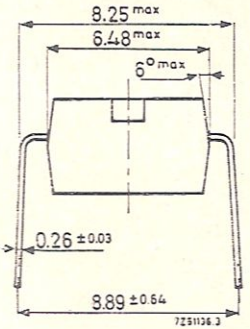
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

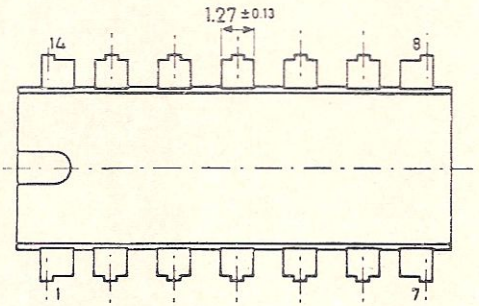
PACKAGE OUTLINE

XG14; dual in-line.

Dimensions in mm







A) The spacing between centerlines of any two pins is equal to the true position spacing of 2.54 mm per pin with a total tolerance of ± 0.25 mm.

Handling notes

1. Devices may be soldered directly into circuits with soldering irons. At iron temperatures below 245 °C the maximum soldering time should be less than 10 seconds and at iron temperatures between 245 °C and 400 °C the soldering time should be less than 5 seconds. In both cases the soldering iron should be applied below the seating plane (see outline drawing).

2. Devices mounted up to the seating plane on a printed circuit board may be dip or flow soldered providing the solder temperature is below 245 °C and the time of immersion is less than 5 seconds. The body temperature should not be allowed to exceed the maximum storage temperature during soldering. If excessive preheat cycles are used, it may be necessary to cool the printed board immediately after leaving the solder bath/wave in order that this requirement is met.